ABSTRACT OF THE DISCLOSURE

A CPU and a memory are connected to each other through an address bus, a data bus, a read signal line and a write signal line. A read control signal and a write control signal transferred to the read signal line and the write signal line, respectively, are supplied to a control signal generating circuit. The control signal generating circuit detects a change in the read control signal and the write control signal transmitted to the read signal line and the write signal line, respectively, and then generates a control signal. The control signal generated by the control signal generating circuit is supplied to a pseudo-data generating circuit. The pseudo-data generating circuit generates pseudo-data comprising any random number data in accordance with the control signal and outputs the pseudo-data onto the data bus.